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EXAMINER	
BODDIE, WILLIAM	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,939	PARK, JIN-HO	
	Examiner	Art Unit	
	WILLIAM L. BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, May 21st, 2008, the Applicant amended claims 1, 7, 12 and added new claims 15-16. Currently claims 1-16 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 21st, 2008 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection. Specifically all of the Applicant's arguments are directed to new limitations and are believed to be answered by new rejection grounds which follow.

Claim Objections

4. Claim 12 is objected to because of the following informalities: lines 9-10 state in part, "the data and gate drivers." Prior to this phrase there is no mention of data and gate drivers. It appears the Applicant might have intended 'a data and gate drivers' or 'data and gate drivers'. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US 5,592,199) in view of Kubota et al. (US 6,791,526) and further in view of Nakamura et al. (US 7,136,058).

With respect to claim 1, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (20 in fig. 1) displaying images (col. 15, lines 27-42) and including:

a first substrate (1 in fig. 1), and a second substrate facing the first substrate (2 in fig. 1);

gate lines (x-axis 3 in fig. 1, for example) disposed on the second substrate and opposing the first substrate (fig. 1), the gate lines receiving a gate driving signal; and

an output instruction signal line (73 in figs. 1-3) disposed on the second substrate (fig. 1) transmitting an output instruction signal;

a data driver (3 y-axis ICs, 5 in fig. 1) outputting image data to the LCD panel;

a gate driver (2 x-axis ICs, 5 in fig. 1) outputting a gate driving signal to the LCD panel; and

a timing controller (8 in fig. 1; col. 19, lines 15-18) providing a first control signal (x-axis 73 in fig. 1) to the gate driver so as to control an output of the gate driving signal and providing the output instruction signal (y-axis 73 in fig. 1) to the data driver via the

output instruction signal line so as to control an output of the image data (col. 25, lines 3-12),

wherein the gate line and the output instruction signal line are disposed substantially parallel to each other (gate lines are seen as the parallel lines that are output from 2 x-axis ICs, 5 in fig. 1, into the panel, while the output instruction signal lines are seen as the 73 wiring that connects the y-axis ICs; should be clear from fig. 1 that these two sets of lines are parallel to one another) on the second substrate (fig. 3), and

wherein the output instruction signal line is substantially a same length as the gate lines (from figs. 2-3, it is clear that 73 spans substantially the entire length of the LCD panel just as the gate lines do).

Kawaguchi does not expressly disclose, that the timing of the output of image data is according to a delay of the gate driving signal.

Kubota discloses, that the timing of the output of image data (input and shift register waveforms in fig. 18) is according to a delay of a gate driving signal (output in fig. 18).

Kubota and Kawaguchi are analogous art because they are both from the same field of endeavor namely control circuitry design for LCD panels.

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

Neither Kubota nor Kawaguchi expressly discloses a common electrode disposed on the first substrate; or that the output instruction signal line opposes the common electrode.

Nakamura discloses, an LCD apparatus comprising:

a first substrate, and a second substrate facing the first substrate (col. 4, lines 10-19);

a common electrode disposed on the first substrate (col. 4, lines 17-19);

gate lines disposed on the second substrate and opposing the common electrode (col. 4, lines 10-19); and

signal lines (P1 in fig. 14; and C4, C5 wiring in fig. 15) disposed on the second substrate and opposing the common electrode such that the signal lines have a capacitive load (fig. 14-15; the signal lines will inherently have a capacitive load due to being overlapped with the common electrode in a manner identical to the Applicant's invention).

Nakamura and Kawaguchi are analogous art because they are both from the same field of endeavor, namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the output instruction signal lines of Kawaguchi and Kubota so as to overlap the common electrode as taught by Nakamura.

The motivation for doing so would have been to reduce the frame size of the LCD, resulting in a more portable display (Nakamura; col. 15, lines 42-50).

With respect to claim 2, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 1 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is formed on an area adjacent to the data driver (clear from fig. 1).

With respect to claim 3, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 2 (see above).

Kawaguchi further discloses, comprising a plurality of signal transmission members (45 and 3 in fig. 3; for example) electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives the output instruction signal from timing controller via one of the signal transmission members (clear from figs. 1-2).

With respect to claim 4, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 3 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises:

the gate lines (note the outputting gate lines from the y-axis ICs in fig. 1) receiving the gate driving signal via the gate driver, the gate lines disposed on the LCD panel, extended in a first direction and arranged in a second direction substantially perpendicular to the first direction (fig. 1); and

a plurality of data lines (x-axis 3 in fig. 1) receiving the image data via the data driver, the data lines disposed on the LCD panel, extended in the second direction and

arranged in the first direction (col. 37, lines 29-42, discusses the orientation and design of a matrix panel using the gate and data lines oriented in the way currently claimed).

With respect to claim 5, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 4 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is extended in the first direction and is substantially parallel to the gate lines (seems clear from figs. 1-3).

With respect to claim 6, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 4 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area (col. 1, lines 62-67).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

With respect to claim 7, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (20 in fig. 1) displaying images (col. 15, lines 27-42) and including:

a first substrate (1 in fig. 1), and a second substrate facing the first substrate (2 in fig. 1);

gate lines (x-axis 3 in fig. 1, for example) disposed on the second substrate and opposing the first substrate (fig. 1), the gate lines receiving a gate driving signal; and

an output instruction signal line (73 in figs. 1-3) disposed on the second substrate (fig. 1) transmitting an output instruction signal;

a data driver (3 y-axis ICs, 5 in fig. 1) outputting image data to the LCD panel;

a gate driver (2 x-axis ICs, 5 in fig. 1) outputting a gate driving signal to the LCD panel; and

a timing controller (8 in fig. 1; col. 19, lines 15-18) providing a first control signal (x-axis 73 in fig. 1) to the gate driver so as to control an output timing of the gate driving signal and providing the output instruction signal (y-axis 73 in fig. 1) to the data driver so as to control an output timing of the image data; and

a plurality of signal transmission members (45 and 3 in fig. 3; for example) electrically connecting the data driver with the LCD panel;

wherein the output instruction signal line provides the output instruction signal to the data driver via one of the signal transmission members (clear from figs. 1-3); and

wherein the gate line and the output instruction line are disposed substantially parallel to each other (gate lines are seen as the parallel lines that are output from y-axis ICs in fig. 1 into the panel, while the output instruction signal lines are seen as the 73 wiring that connects the ICs; should be clear from fig. 1 that these two sets of lines are parallel to one another) on the second substrate (fig. 3), and

wherein the output instruction signal line is substantially a same length as the gate lines (from figs. 2-3, it is clear that 73 spans substantially the entire length of the LCD panel just as the gate lines do).

Kawaguchi does not expressly disclose, that the timing of the output of image data is according to a delay of the gate driving signal.

Kubota discloses, that the timing of the output of image data (input and shift register waveforms in fig. 18) is according to a delay of a gate driving signal (output in fig. 18).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

Neither Kubota nor Kawaguchi expressly discloses a common electrode disposed on the first substrate; or that the output instruction signal line opposes the common electrode.

Nakamura discloses an LCD apparatus comprising:

a first substrate, and a second substrate facing the first substrate (col. 4, lines 10-19);

a common electrode disposed on the first substrate (col. 4, lines 17-19);

gate lines disposed on the second substrate and opposing the common electrode (col. 4, lines 10-19); and

signal lines (P1 in fig. 14; and C4, C5 wiring in fig. 15) disposed on the second substrate and opposing the common electrode such that the signal lines have a capacitive load (fig. 14-15; the signal lines will inherently have a capacitive load due to being overlapped with the common electrode in a manner identical to the Applicant's invention).

Nakamura and Kawaguchi are analogous art because they are both from the same field of endeavor namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the output instruction signal lines of Kawaguchi and Kubota so as to overlap the common electrode as taught by Nakamura.

The motivation for doing so would have been to reduce the frame size of the LCD, resulting in a more portable display (Nakamura; col. 15, lines 42-50).

With respect to claim 8, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 7 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises:

the gate lines (note the outputting gate lines from the ICs in fig. 1) extended in a first direction and arranged in a second direction substantially perpendicular to the first direction; and

a plurality of data lines (x-axis 3 in fig. 1) extended in the second direction and arranged in the first direction (col. 37, lines 29-42, discusses the orientation and design of a matrix panel using the gate and data lines oriented in the way currently claimed).

With respect to claim 9, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 8 (see above).

Kawaguchi further discloses, wherein the output instruction line is extended in the first direction (clear from fig. 1).

With respect to claim 10, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 9 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal and the image data are substantially simultaneously provided to a corresponding pixel area (col. 1, lines 62-67).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

With respect to claim 11, Kawaguchi, Nakamura and Kubota disclose, the LCD apparatus of claim 7 (see above).

Kawaguchi further discloses, wherein the signal line is formed on the LCD panel and adjacent to the data driver (clear from fig. 1).

With respect to claim 15, Kawaguchi, Nakamura and Kubota disclose the LCD apparatus of claim 1 (see above).

Kawaguchi, when combined with Nakamura and Kubota, further discloses wherein capacitive and resistive loads of the gate lines and the output instruction signal line are substantially equal to each other (Kawaguchi discloses that the output instruction line and the gate lines are formed on the same substrate. This is seen as sufficient to generate capacitive and resistive loads that are substantially equal to one another. As discussed by the Applicants on page 13, lines 16-23, all that is attributed to the two lines have equal loads is that they be formed on the same substrate).

With respect to claim 16, Kawaguchi, Nakamura and Kubota disclose the LCD apparatus of claim 1 (see above).

Kawaguchi, when combined with Nakamura and Kubota, further discloses wherein a delay of providing the output instruction signal to the data driver is substantially equal to the delay of the gate driving signal (Kawaguchi discloses that the output instruction line and the gate lines are formed on the same substrate. This is

seen as sufficient to delay the two signals an equal amount. As discussed by the Applicants on page 13, lines 16-23, all that is attributed to the two lines having equal delays is that they be formed on the same substrate).

7. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US 5,592,199) in view of Nakamura et al. (US 7,136,058).

With respect to claim 12, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (20 in fig. 1) displaying images (col. 15, lines 27-42) including:

a first substrate (1 in fig. 1), and a second substrate facing the first substrate (2 in fig. 1);

gate lines (x-axis 3 in fig. 1, for example) disposed on the second substrate and opposing the first substrate (fig. 1) receiving a gate driving signal;

an output instruction signal line (73 in fig. 1) disposed on the second substrate (73 in fig. 1) the output instruction signal line electrically connecting the timing controller with the data and gate drivers (col. 19, lines 15-18; details the timing control board supplying signal along the circuitry of the device to the drivers. The output instruction signal line is one part of this circuitry and as such is seen as electrically connecting the timing controller with the data and gate drivers);

a data driver coupled to the LCD panel (3 y-axis ICs, 5 in fig. 1);

a gate driver coupled to the LCD panel (2 x-axis ICs, 5 in fig. 1);

a timing controller coupled (8 in fig. 1; col. 23, lines 29-40) to the gate driver and to the data driver; and

wherein the gate line and the output instruction signal line are disposed substantially parallel to each other (gate lines are seen as the parallel lines that are output from 2 x-axis ICs, 5 in fig. 1, into the panel, while the output instruction signal lines are seen as the 73 wiring that connects the y-axis ICs; should be clear from fig. 1 that these two sets of lines are parallel to one another) on the second substrate (fig. 3); and

wherein the output instruction signal line is substantially a same length as the gate lines (from figs. 2-3, it is clear that 73 spans substantially the entire length of the LCD panel just as the gate lines do).

Kawaguchi does not expressly disclose a common electrode disposed on the first substrate; or that the output instruction signal line opposes the common electrode.

Nakamura discloses, an LCD apparatus comprising:

a first substrate, and a second substrate facing the first substrate (col. 4, lines 10-19);

a common electrode disposed on the first substrate (col. 4, lines 17-19);

gate lines disposed on the second substrate and opposing the common electrode (col. 4, lines 10-19); and

signal lines (P1 in fig. 14; and C4, C5 wiring in fig. 15) disposed on the second substrate and opposing the common electrode such that the signal lines have a capacitive load (fig. 14-15; the signal lines will inherently have a capacitive load due to being overlapped with the common electrode in a manner identical to the Applicant's invention).

Nakamura and Kawaguchi are analogous art because they are both from the same field of endeavor namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the output instruction signal lines of Kawaguchi so as to overlap the common electrode as taught by Nakamura.

The motivation for doing so would have been to reduce the frame size of the LCD, resulting in a more portable display (Nakamura; col. 15, lines 42-50).

With respect to claim 13, Kawaguchi and Nakamura disclose, the LCD apparatus of claim 12 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is formed on an area adjacent to the data driver (clear from fig. 1).

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US 5,592,199) in view of Nakamura et al. (US 7,136,058) and further in view of Kubota et al. (US 6,791,526).

With respect to claim 14, Kawaguchi and Nakamura disclose, the LCD apparatus of claim 13 (see above).

Kawaguchi further discloses a plurality of signal transmission members (45 and 3 in fig. 3; for example) electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives a control signal from the timing controller via one of the signal transmission members so as to control an output of an image data from the data driver (col. 23, lines 29-40; clear from figs. 1-2).

Neither Nakamura nor Kawaguchi expressly disclose, that the timing of the output of image data is according to a delay of the gate driving signal.

Kubota discloses, that the timing of the output of image data (input and shift register waveforms in fig. 18) is according to a delay of a gate driving signal (output in fig. 18).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William L Boddie/
Examiner, Art Unit 2629
7/29/08

/Sumati Lefkowitz/
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